PATENT

Confirmation No. 1784

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	VAN DAL *et al.*	Examiner:	Ingham, John C.
Serial No.:	10/575,288	Group Art Unit:	2814
Filed:	April 11, 2006	Docket No.:	NL031259US1 (NXPS.548PA)
Title:	SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING SUCH A SEMICONDUCTOR DEVICE		

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Respectfully submitted,

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NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
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APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Customer No.
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Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed March 13, 2009 and in response to the rejections of claims 1-2, 4-6 and 8-13 as set forth in the Final Office Action dated November 17, 2008.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 017784/0816 to NXP, B.V., headquartered in Eindhoven, the Netherlands.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-2, 4-6 and 8-13 stand rejected and are presented for appeal. Claims 3 and 7 are cancelled. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

No amendments have been filed subsequent to the Final Office Action dated November 17, 2008.

V. Summary of Claimed Subject Matter

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided below. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified below, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and references the appended claims and their legal equivalents for a complete statement of the invention.

As consistent with example embodiments relevant to claim 1, a semiconductor device includes a substrate and a semiconductor body of silicon, which includes a field effect

transistor having a source region that borders on the surface of the semiconductor body and that is connected to a lower-doped, thinner source region extension and having a drain region that borders on the surface of the semiconductor body. The drain region is similarly connected to a lower-doped, thinner drain region extension, with the regions and extensions being of a first conductivity type. *See, e.g.*, device 10 of FIG. 6, with body 1, FET 3, source region 2, drain region 3 and extension regions 2A, 3A as described at paragraphs 0022-0026. The source region and the source region extension, and the drain region and the drain region extension are respectively connected with each other via an intermediate region of the first conductivity type and having a thickness and doping concentration that ranges between those of the region and the extension which are connected with one another by the intermediate region. *See, e.g.*, device 10 of FIG. 6 as discussed above, with intermediate regions 2C, 3C and corresponding description at paragraphs 0006 and 0024. A channel region is situated between the drain regions and extensions, and is of a second conductivity type that is opposite to the first conductivity type (*see* FIG. 6 as above). A gate electrode is separated from the channel region by a dielectric region, with each of the gate electrode, the source region and the drain region being provided with respective connection regions containing a metal silicide (*see, e.g.,* 8 in FIG. 6 as described above, with resulting regions 2B, 3B as in FIG. 1). A sloped spacer of an electrically insulating material is situated on the semiconductor body on either side of the gate electrode and directly contacting the intermediate region and the associated extension (*see* FIG. 6 as above and paragraph 0022).

As consistent with example embodiments relevant to claim 5, a method of manufacturing a semiconductor device includes forming such a device with a substrate and a semiconductor body of silicon that includes a field effect transistor (*see, e.g.*, FIG. 6 and paragraphs 0022- 0026 describing body 1, FET 3). A dielectric region is formed on the channel region, a gate electrode is formed on the dielectric, and a spacer of an electrically insulating material is formed on either side of the gate electrode (*see, e.g.*, FIG. 6 and 4, 5 6 and 7). At the surface of the semiconductor body, a source region is formed, and an intermediate region is formed by an ion implantation of a doping element of the first conductivity type, the ion implantation being carried out at an acute angle with the normal to the surface of the semiconductor body (*see, e.g.*, FIG. 6 and 2/2C and 3/3C, as described at

paragraph 0022-0023). Lower-doped, thinner source region extension and drain region extension are formed of a first conductivity type, with the channel region between the extensions being of a second conductivity type, opposite to the first conductivity type (*see*, *e.g.*, source extension 2A and drain extension 3A in FIG. 6, and paragraph 0011). The source region and the drain region are provided with a connection region which comprises a metal silicide (*see*, *e.g.*, FIG. 6 and 8, with resulting regions 2B, 3B in FIG. 1). The intermediate region is provided with a thickness and a doping concentration which range between those of the region and the extension which are connected to one another by the intermediate region (*see*, *e.g.*, device 10 of FIG. 6 as discussed above, with intermediate regions 2C, 3C and corresponding description at paragraphs 0006 and 0024).

VI. Grounds of Rejection to be Reviewed Upon Appeal

The grounds of rejection to be reviewed on appeal are as follows:

A. Claims 1-2, 4-6, 8 and 10-13 stand rejected under 35 U.S.C. § 103(a) over the Wang reference (U.S. Patent No. 5,686,324) and a "Chao" reference (no citation given).

B. Claim 9 stands rejected under 35 U.S.C. § 103(a) over the Wang and Chao references in further view of a "Yu" reference (no citation given).

VII. Argument

As discussed in Applicant's response to the Final Office Action, the referenced "Chao" and "Yu" references were not identified (*i.e.*, by any serial number, patent number or publication reference). While Appellant believes that this failure to identify the references rendered the rejections as well as the finality of the Office Action improper, Appellant has based the following remarks upon an understanding from the Advisory Action's indication that the reference to "Chao" is to U.S. Patent No. 4,818,715 and to "Yu" is to U.S. Patent No. 6,225,176, while maintaining that the rejections are improper. Appellant further believes that this issue is not relevant because the § 103(a) rejections involving these references are improper, as discussed in the following.

A. The § 103(a) Rejection of Claims 1-2, 4-6, 8 And 10-13 Over The '324 And '715 References Should Be Reversed

1. The Rejection Should Be Reversed Because The Proposed Modification Of The '324 Reference Renders The Reference Inoperable For Its Purpose

The § 103 (a) rejections of claims 1-2, 4-6, 8 and 10-13 are improper because the (final) Office Action's proposed modification of the primary '324 reference to include the self-aligned silicide (salicide) shown in FIG. 5i of the '715 reference would render the '324 reference inoperable for its purpose involving combined (concurrent) etch/formation steps as stated initially in the Abstract and repeated throughout the disclosure of the '324 reference. As such, the '324 reference cannot be modified to correspond to the claimed invention, and the cited references further teach away from the proposed modification, as the combined etch/formation steps would be separated. When the prior art teaches away and/or renders the reference being modified unsatisfactory for its intended purpose, the law is clear that there is no motivation to support an obviousness rejection. *See, e.g.,* M.P.E.P. §§ 2143.01 (citing *In re Gordon*, 733 F.2d 900 (Fed. Cir. 1984)) (a § 103 rejection cannot be maintained when the asserted modification undermines purpose of the main reference)); and *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727 (U.S. 2007).

In this instance, the '324 reference requires that insulating layers be formed over the gate and source/drain regions prior to the formation of source and drain contacts (*see*, *e.g.*, cited FIG. 19 as well as related FIG. 22, and the respective NSG and BPSG layers, with FIG. 22 copied below for convenience.

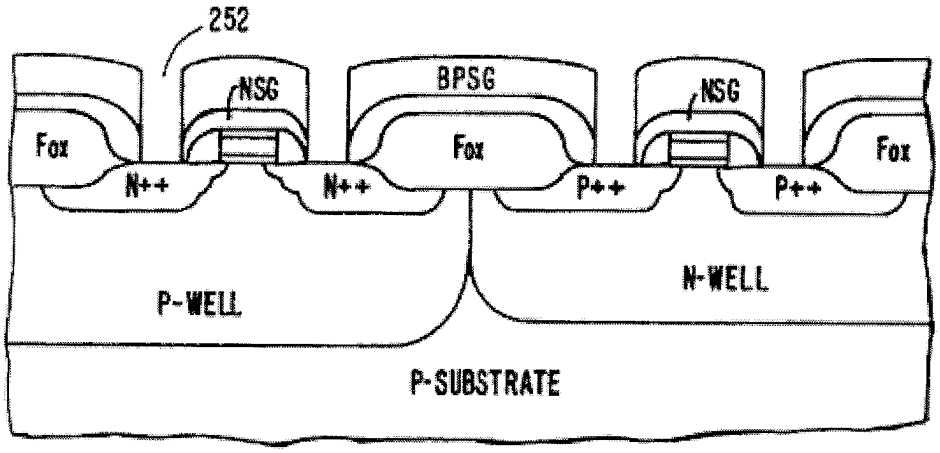


FIG. 22.

As part of the '324 reference's stated purpose of reducing the number of steps (see column 6:18-22), the '324 reference combines the step of forming source/drain contacts with the step of forming vias 252 in the insulating NSG and PBSG layers (*see* FIG. 22). The '324 reference achieves this purpose, for example, by etching vias 252 and preparing the source/drain regions for contacts in a process where "the top surface of each source/drain region is 'cleared' from oxides before applying contact metallization" (*see*, *e.g.*, column 8:54-57).

Accordingly, the '324 reference teaches away from the proposed modification because forming self-aligned silicide on the respective gate, source and drain contacts in the '324 reference would undermine the aforesaid stated purpose in requiring additional steps, prior to forming the NSG and PBSG layers. That is, rather than form the contacts in connection with via formation, separate steps would need to be carried out to remove oxide and expose the source, drain and gate regions for self-alignment thereto. Additional steps would need to be carried out in order to deposit metal at the exposed regions, and to

subsequently heat-treat related heat treatment for salicidation. The step of forming via openings 252 would still need to be carried out, as would the deposition (*e.g.*, of metal) to form the vias themselves. Correspondingly, the proposed modification of the '324 reference would add steps to remove oxide from the respective gate, remove oxide from the source and remove oxide from the drain. Ostensibly, additional steps would then be carried out to form a metal contact layer. Appellant submits that such additional steps, where the '324 reference already provides contact regions (using fewer steps) and expressly identifies its purpose as avoiding such additional steps, is contrary to the M.P.E.P. and relevant law. Appellant therefore requests that the rejections be reversed.

2. The Cited Combination Does Not Disclose All Claim Limitations

The Section 103 rejections are also improper because they fail to provide teaching or suggestion of all claim limitations. For instance, the cited portions of the '715 reference do not teach or suggest multiple claim limitations, including those directed to a recessed, silicide contact at a source and drain region, and to a similar contact at a gate region. These limitations are described by way of example in Appellant's specification at paragraph 0007, which describes the recessed metal silicide "formed by reaction of a metal deposited on the semiconductor body and the underlying silicon of the semiconductor body." FIG. 6 and FIG. 1 respectively exemplify related embodiments, showing recessed silicide regions 2B, 3B (in FIG. 1), formed from what is shown in FIG. 6 as relevant, for example, to the embodiments described at paragraph 0021. For convenience, Appellant has respectively copied Figures 6 and 1 below, with the recessed silicide regions 2B, 3B and 6B formed using deposited metal layer 8, (*e.g.*, in a high-temperature thermal treatment as described at paragraph 0025).

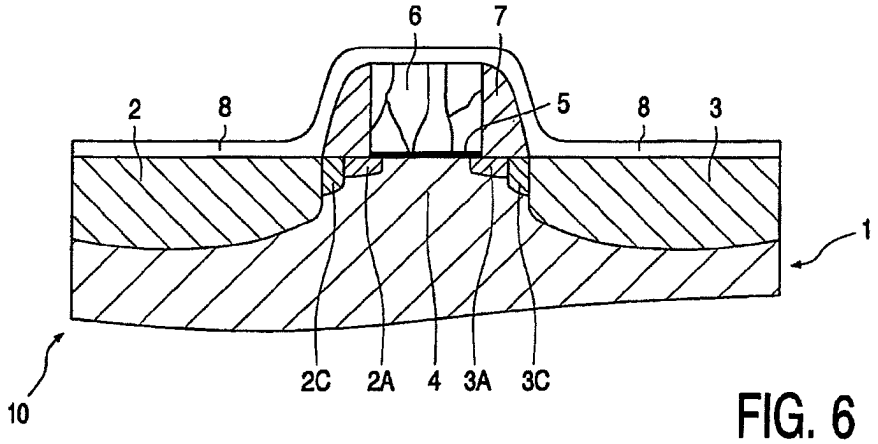


FIG. 6

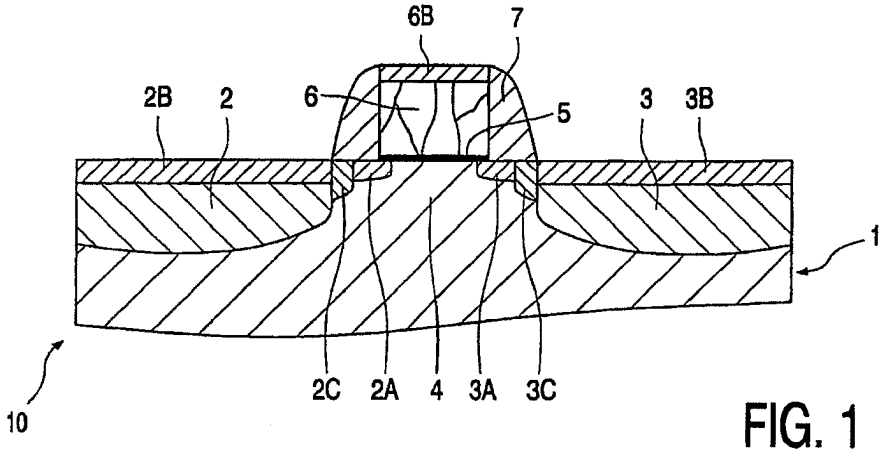
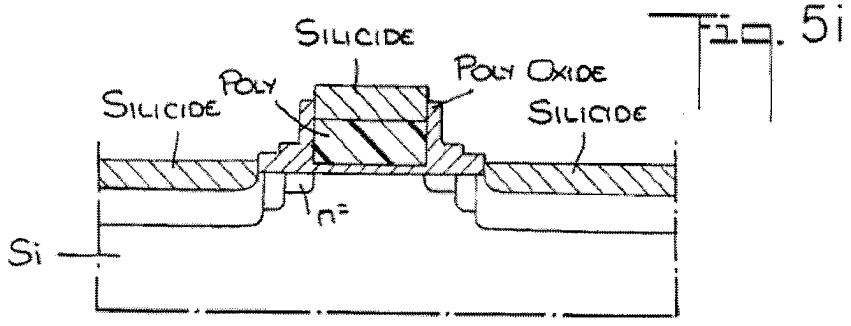


FIG. 1

In contrast to FIG. 1 and the related discussion above, the cited portions of the '715 reference (FIG. 5i) show a silicide contact that extends well above the surface of all three of the gate, source and drain. FIG. 5i is copied below for convenience.



As shown above in FIG. 5i of the '715 reference, the silicide region extends above the respective source and drain regions, along a lower portion of a stepped poly oxide spacer. Accordingly, this silicide region is not recessed in the source and drain regions as claimed, and thus fails to correspond to related claim limitations including those in claim 2 directed to limitations wherein "the connection region is recessed in the semiconductor body." Appellant therefore requests that the § 103 rejections be reversed for failing to provide teaching or suggestion of all claim limitations.

3. The Rejection Must Be Reversed Because The Office Action Failed To Identify The "Chao" Reference

All of the claim rejections as newly-presented in the Office Action are also improper because the Office Action did not provide any citation that identifies the cited "Chao" reference. This failure to identify the "Chao" reference renders the rejection insufficient for establishing and maintaining any rejection under § 103. The Advisory Action indicates that this reference was made of record earlier (5.16.08); however, as the Office Action did not specify which "Chao" reference was being referred to, the rejections as made therein were improper. In the event that any rejections of claims 1-2, 4-6, 8 and 10-13 are not reversed for other reasons stated herein, Appellant requests that prosecution be reopened and further that the Appellant be afforded an opportunity to further assess the rejections and to respond.

B. The Rejection Of Claim 9 Over The Proposed Combination Of The '324, '715 And '176 References Should Be Reversed

1. The Rejection Should Be Reversed Because No Reference Has Been Cited As Corresponding To Claim Limitations, And The Asserted Requirements Of "Criticality" Are Contrary To The M.P.E.P. And Applicable Law

The § 103(a) rejection of claim 9 over the '324 and "Chao" references in further view of the '176 reference is improper because the Office Action has failed to cite any evidence in support of the assertion that one of skill in the art would be motivated to modify the '324 reference to include the indicated ion implant energy used in the '176 reference. Moreover, the Office Action has provided no explanation as to how the '324 reference could operate under such conditions. Instead, the Office Action appears to have erroneously relied upon an

assertion that such an implant energy "would have been obvious" without "evidence of disclosure of criticality for the range giving unexpected results."

Appellant submits that such a requirement that the Appellant demonstrate "criticality" or "unexpected results" is inapplicable where no *prima facie* case of obviousness has been presented. For instance, according to M.P.E.P. § 2144.05, such assertions of a lack in criticality of ranges are applicable only where the prior art discloses the relevant conditions without specificity. This is also consistent with case law cited in M.P.E.P. § 2144.05, in which such assertions of lack of criticality are based upon cited art that discloses related ranges (*see, e.g., In re Aller*, 220 F.2d 454, 456 (1955) (a process performed at a temperature between 40°C and 80°C held obvious over a reference which differed in that the reference process was performed at a temperature of 100°C). As applicable here, the Office Action has not asserted that any reference discloses the claimed ion implantation with regard to any range or in any range of energy and flux, much less any such range as relevant to the claimed invention. The Section 103 rejection of claim 9 is therefore improper, and Appellant requests that it be reversed.

2. The Rejection Must Be Reversed Because The Office Action Failed To Identify Either Of The "Chao" Or "Yu" References

The rejection or claim 9 as newly-presented in the Office Action is also improper because the Office Action did not provide any citation that identifies the cited "Yu" reference. This failure to identify the "Yu" reference renders the final rejection insufficient for establishing and maintaining any rejection under § 103. The Advisory Action indicates that this reference was made of record earlier (5.16.08); however, as the Office Action did not specify which "Yu" reference was being referred to, the rejections as made therein were improper. In the event that any rejection of claim 9 is not reversed for other reasons stated herein, Appellant requests that prosecution be reopened and further that the Appellant be afforded an opportunity to further assess the rejections and to respond.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-2, 4-6 and 8-13 are improper and therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

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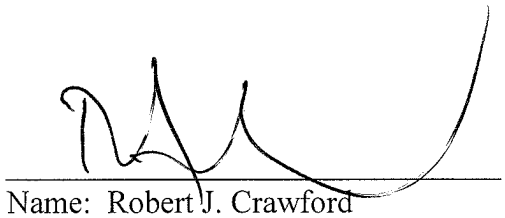
By: 

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 11/575,288)

1. A semiconductor device with a substrate and a semiconductor body of silicon which comprises a field effect transistor having a source region which borders on the surface of the semiconductor body and which is connected to a lower-doped, thinner source region extension and having a drain region which borders on the surface of the semiconductor body and which is connected to a lower-doped, thinner drain region extension, which regions and extensions are of a first conductivity type, and having a channel region situated between said regions and extensions, which channel region is of a second conductivity type, opposite to the first conductivity type, and having a gate electrode separated from the channel region by a dielectric region, each of the gate electrode, the source region and the drain region being provided with respective connection regions containing a metal silicide, characterized in that the source region and the source region extension, and the drain region and the drain region extension are in each case connected with each other via an intermediate region of the first conductivity type the thickness and doping concentration of which range between those of the region and the extension which are connected with one another by the intermediate region, and further wherein a sloped spacer of an electrically insulating material is situated on the semiconductor body on either side of the gate electrode and directly contacting the intermediate region and the associated extension.

2. A semiconductor device as claimed in claim 1, characterized in that the connection region is recessed in the semiconductor body.

4. A semiconductor device as claimed in claim 1, characterized in that the intermediate region is formed by means of ion implantation.

5. A method of manufacturing a semiconductor device with a substrate and a semiconductor body of silicon which comprises a field effect transistor, wherein, at the surface of the semiconductor body, a source region is formed which is connected with a

lower-doped, thinner source region extension and a drain region is formed which is connected with a lower-doped, thinner drain region extension, which regions and extensions are provided with a first conductivity type, and between which a channel region of a second conductivity type, opposite to the first conductivity type, is formed which is provided with a dielectric region on which a gate electrode is formed, and wherein the source region and the drain region are provided with a connection region which comprises a metal silicide, characterized in that an intermediate region of the first conductivity type is formed in each case between the source region and the source region extension and between the drain region and the drain region extension, which intermediate region is provided with a thickness and a doping concentration which range between those of the region and the extension which are connected to one another by the intermediate region, and further characterized in that a spacer of an electrically insulating material is formed on either side of the gate electrode, and the intermediate region is formed by an ion implantation of a doping element of the first conductivity type, the ion implantation being carried out at an acute angle with the normal to the surface of the semiconductor body.

6. A method as claimed in claim 5, characterized in that the metal silicide is formed by providing a metal on the semiconductor body and allowing this metal to react with silicon of the semiconductor body to form the metal silicide of the connection region.

8. A method as claimed in claim 5, characterized in that for the angle at which the ion implantation is carried out an angle between 0 degrees and 45 degrees is chosen.

9. A method as claimed in claim 5, characterized in that the ion implantation is carried out at an energy between 0.5 and 10 keV, and a flux between 5×10^{13} at/cm^2 and 5×10^{14} at/cm^2.

10. A method as claimed in claim 5, characterized in that the source region and the drain region are formed by means of an additional ion implantation, and the intermediate region is

formed immediately before or after the formation of the source region and the drain region, and all these regions are tempered in the same heat treatment.

11. A method as claimed in claim 5, characterized in that the source region extension and the drain region extension are formed by means of an additional ion implantation step.

12. A method as claimed in claim 8, wherein the angle is about 20 degrees to about 40 degrees.

13. A method as claimed in claim 5, wherein the gate electrode is provided with a metal silicide layer.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.